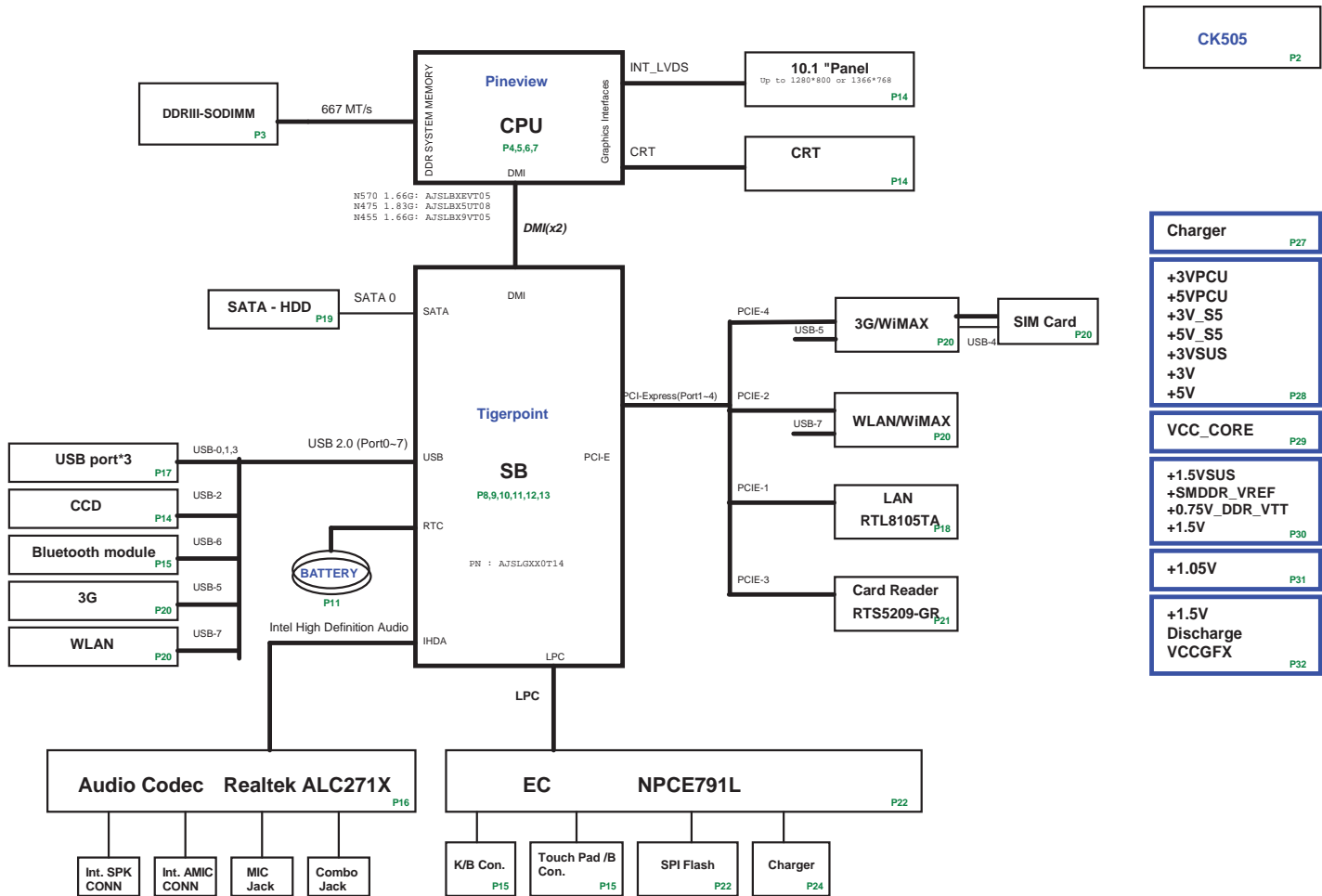
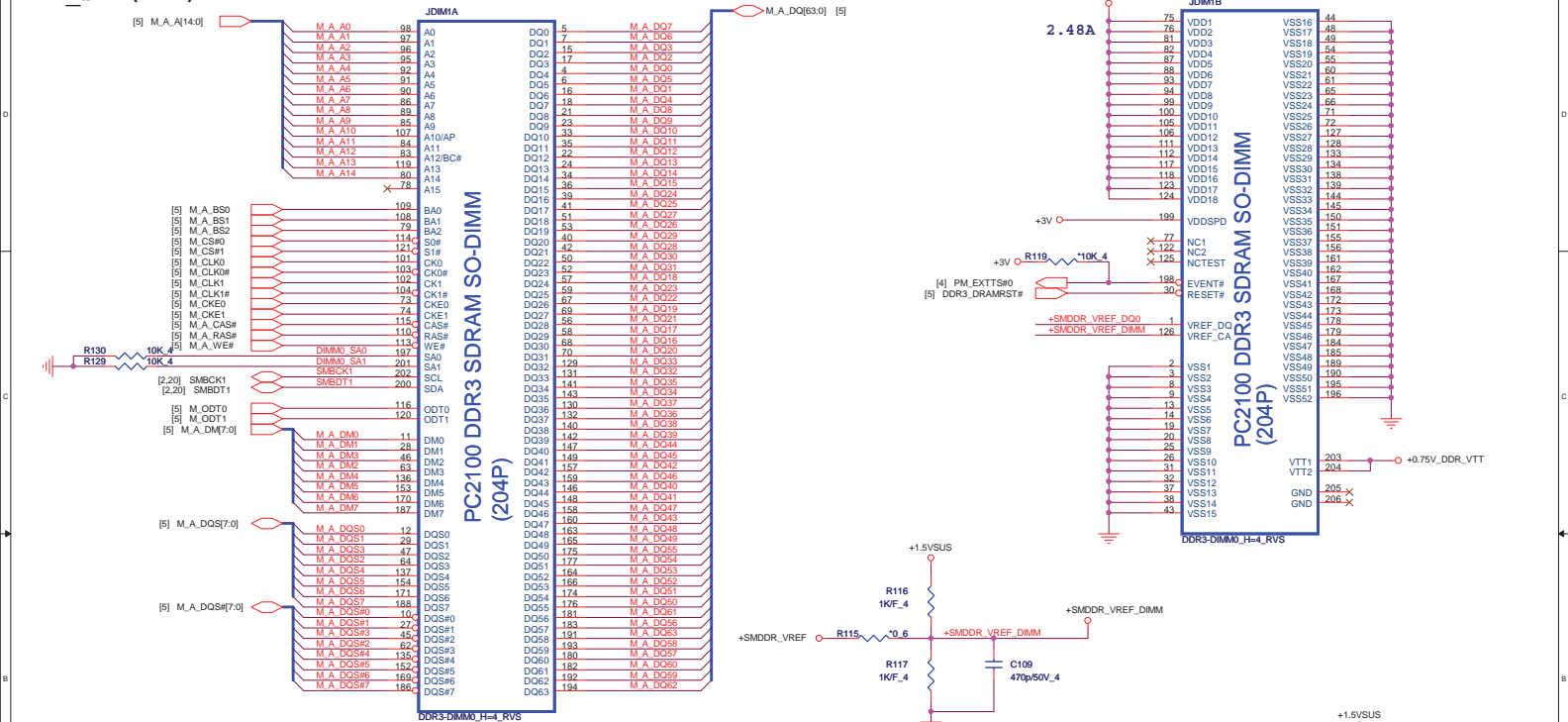


ZE6 Block Diagram

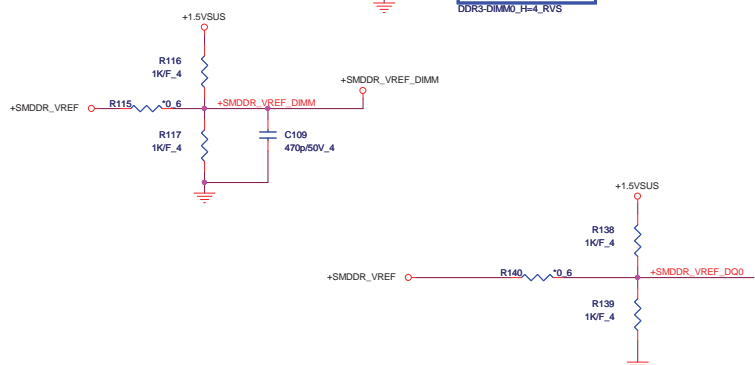
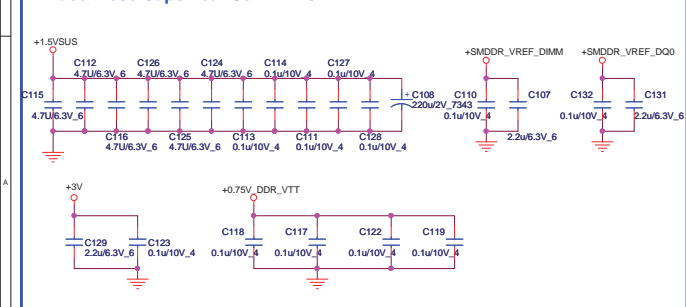




DDR STD (DDR)

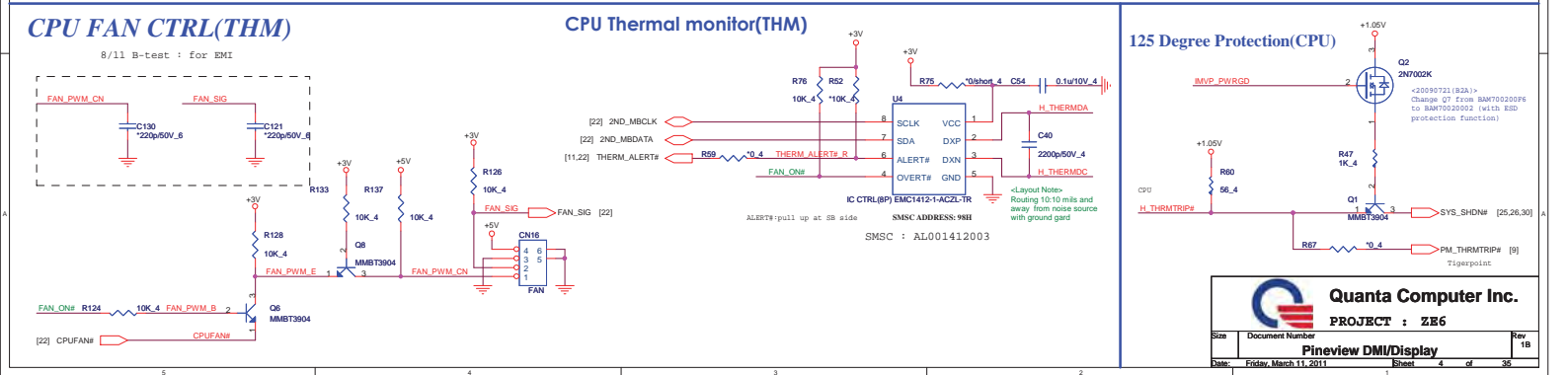


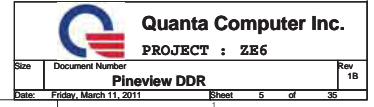
Place these Caps near So-Dimm0.

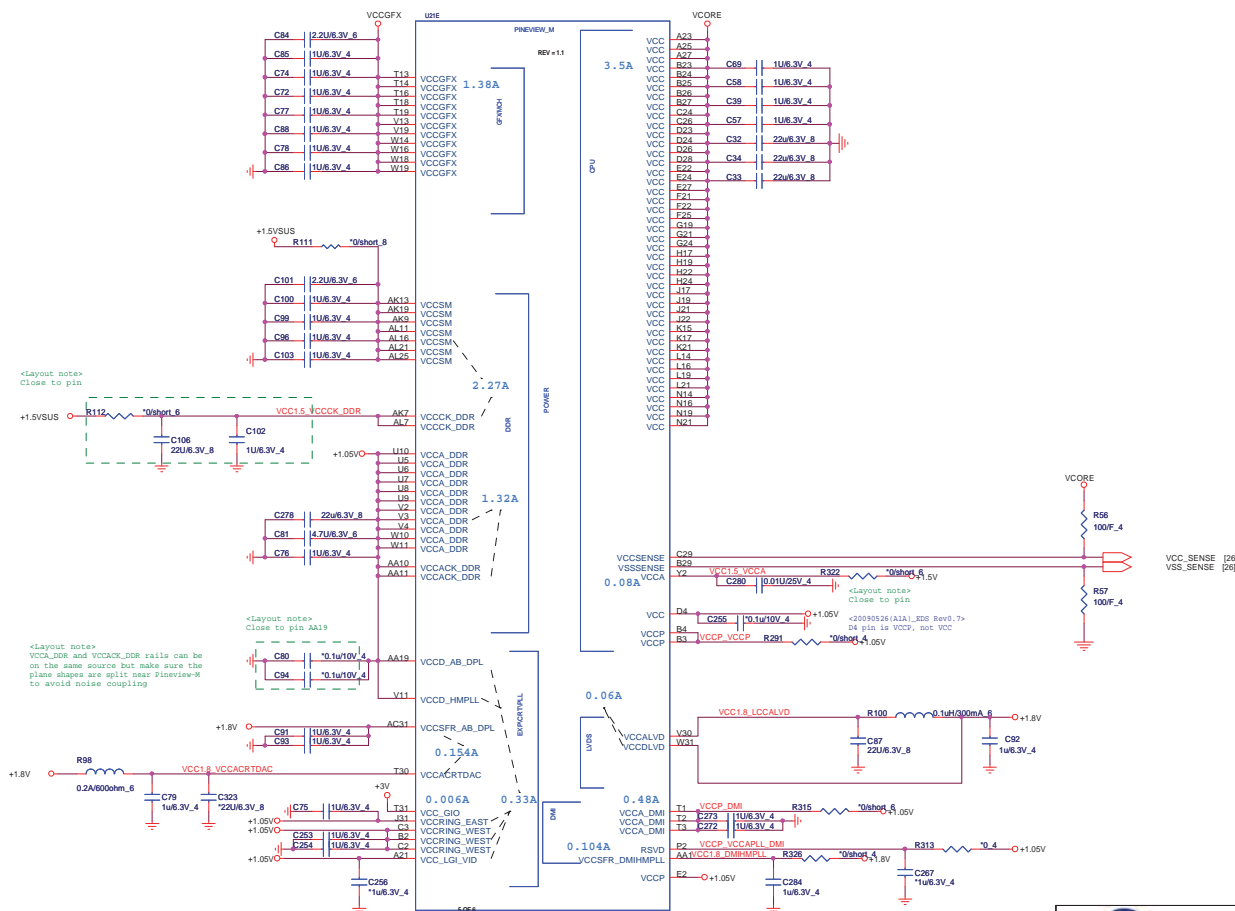
**Quanta Computer Inc.**

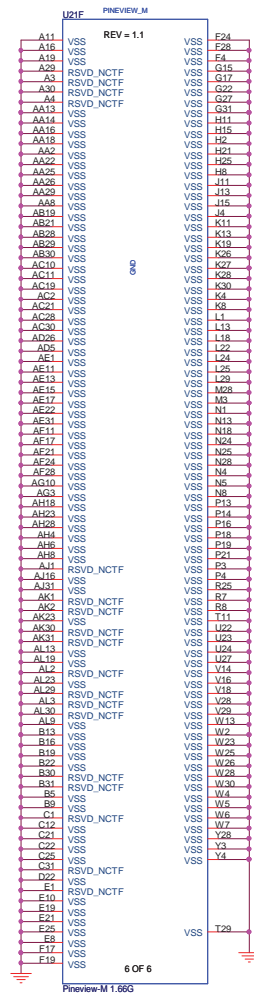
PROJECT : ZE6

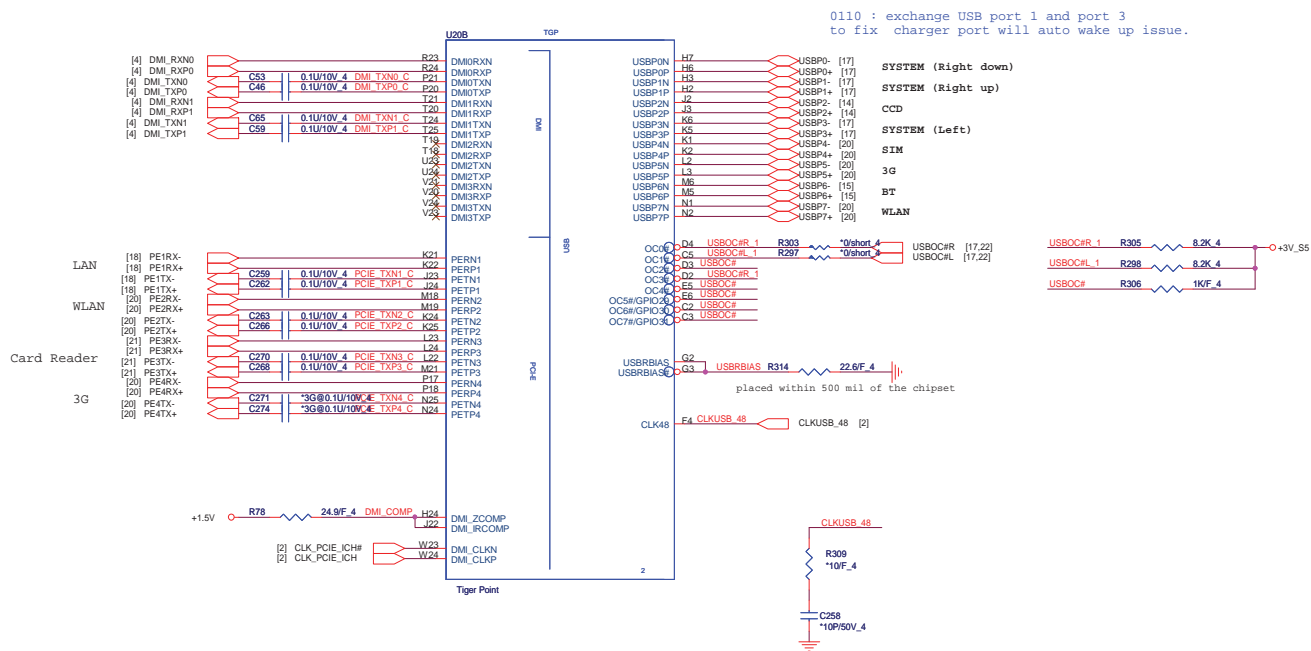
Size	Document Number DDRIII SO-DIMM-0	Rev 1A
Date: Friday, March 11, 2011	Sheet 3 of 35	

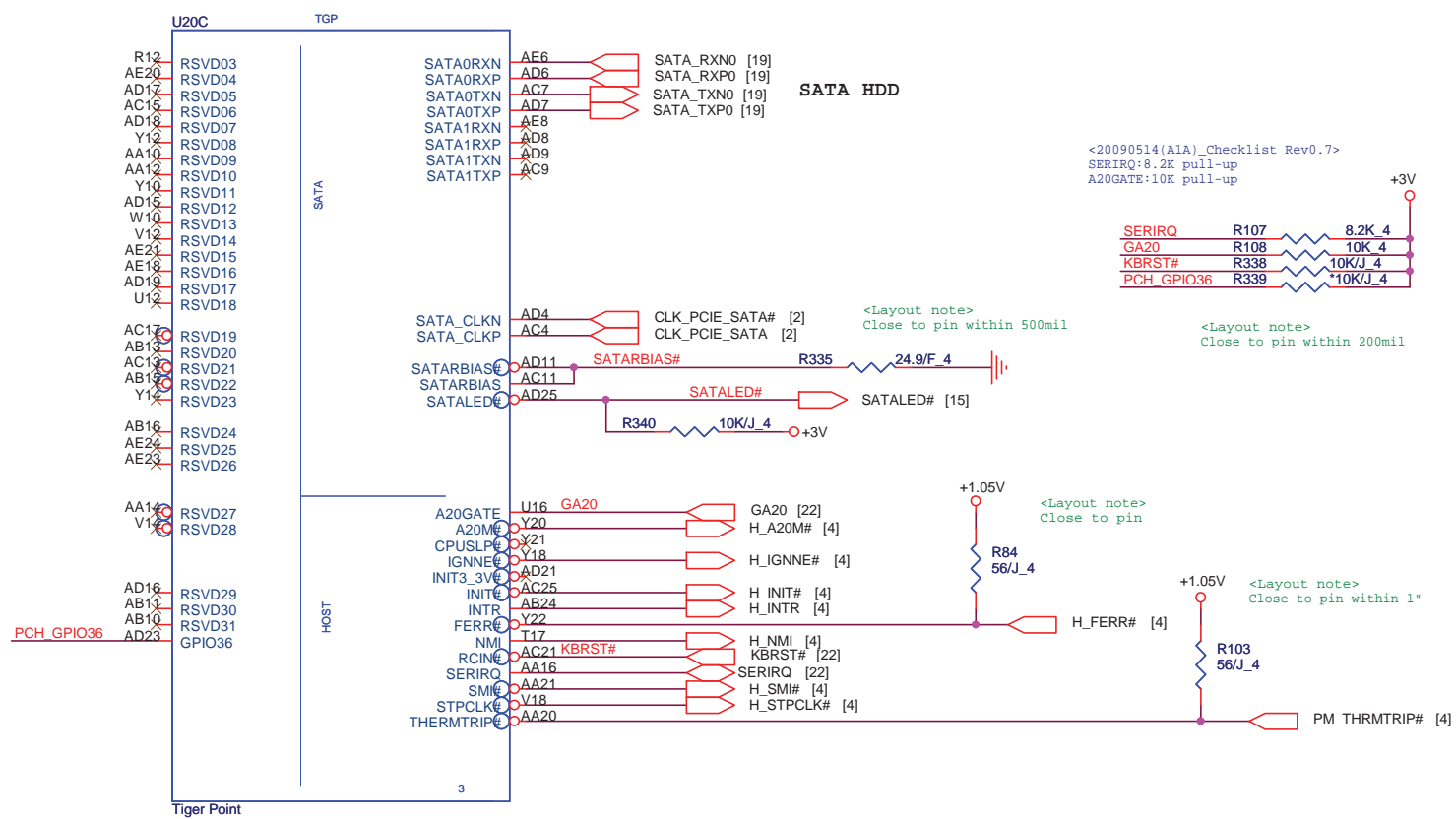













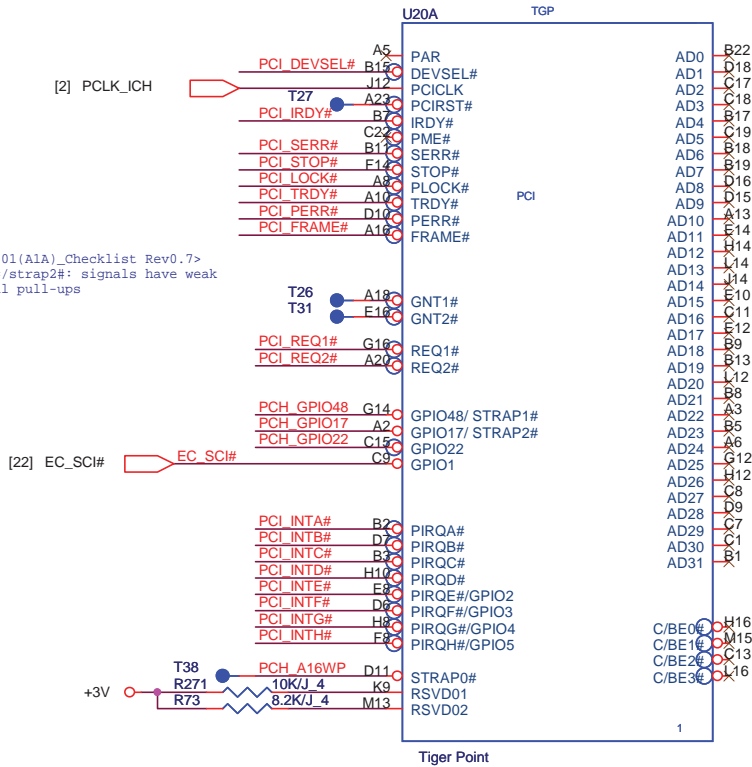
NOTE :
1. CPUSLP# is supported only on nettop platforms.

**Quanta Computer Inc.**

PROJECT : ZE6

Size	Document Number	Rev 1B
Tiger Point Sata/Host		
Date: Friday, March 11, 2011	Sheet 9 of 35	

<20090601(A1A)_Checklist Rev0.7>
Strap1#/strap2#: signals have weak
internal pull-ups



Tiger Point

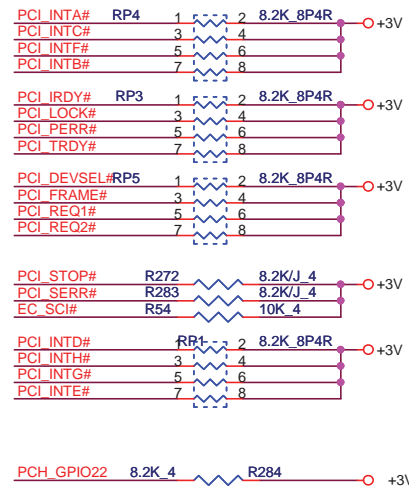
ICH Boot BIOS select

PCH_GPIO17 (INT PU)	PCH_GPIO48 (INT PU)	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (Default)



A16 SWAP Override strap

PCH_A16WP (INT PU)	Low = A16 swap override enabled High = Default
-----------------------	---



IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UH Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2

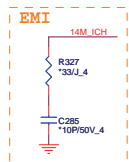
PCI_GNT#2	Internal PU Should not be PD
-----------	---------------------------------



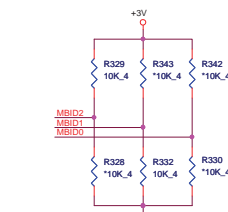
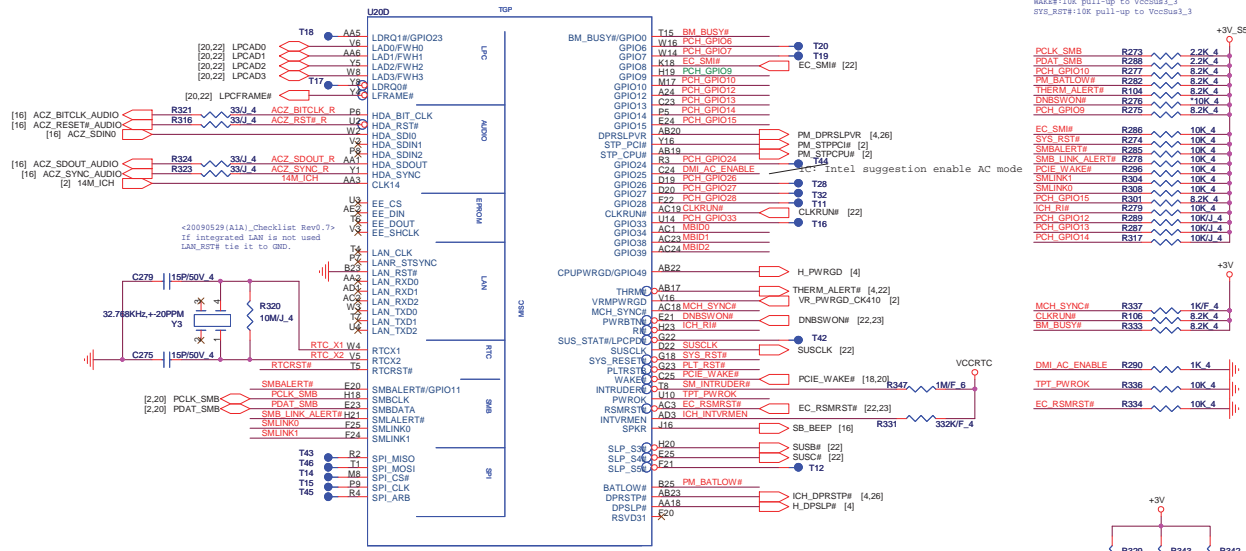
Quanta Computer Inc.

PROJECT : ZE6

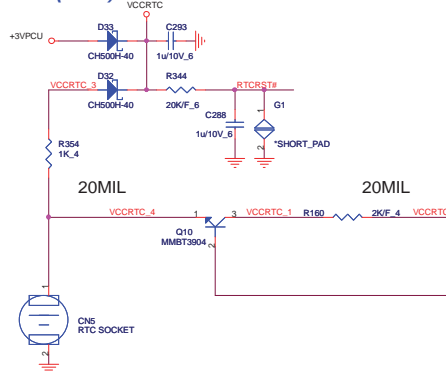
Size	Document Number	Rev 1B
TigerPoint PCI(3/6)		
Date: Friday, March 11, 2011	Sheet 10 of 35	



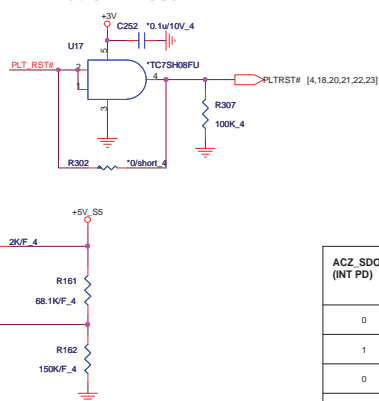
debug port for google require



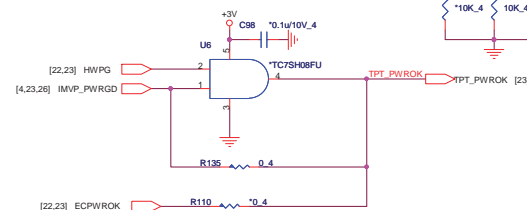
RTC(RTC)



Platform Reset



TPT Power OK



ACZ_SDOUT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0	4 x 1s
1	0	Reserved
0	1	Reserved
1	1	1 x 4s(1 port/4 lanes)

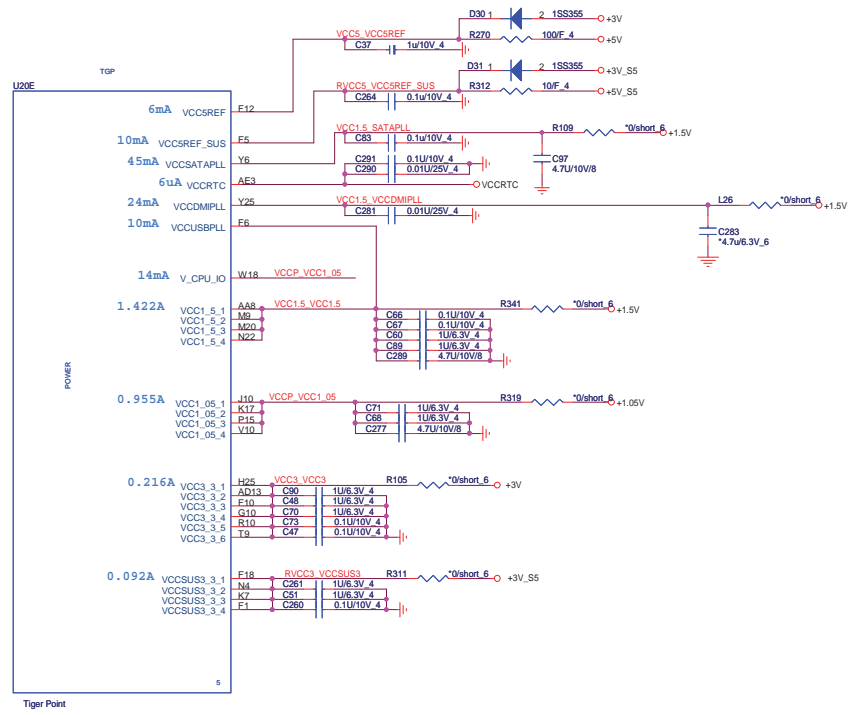
INTVRMEN	
1	Enable internal VccSus1_5 VRM (default)
0	Disable




Quanta Computer Inc.
PROJECT : ZE6

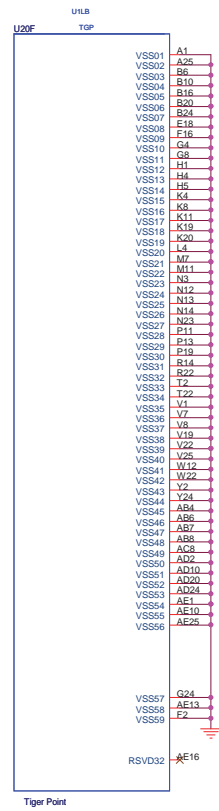
PROJECT : ZE6

<Layout note>
Place 0402 caps close to ball
Place 0603/0805 caps close to ICH




1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

 Quanta Computer Inc. PROJECT : ZE6		Rev
		1B
TigerPoint Power		
Date:	Friday, March 11, 2011	Sheet 12 of 35

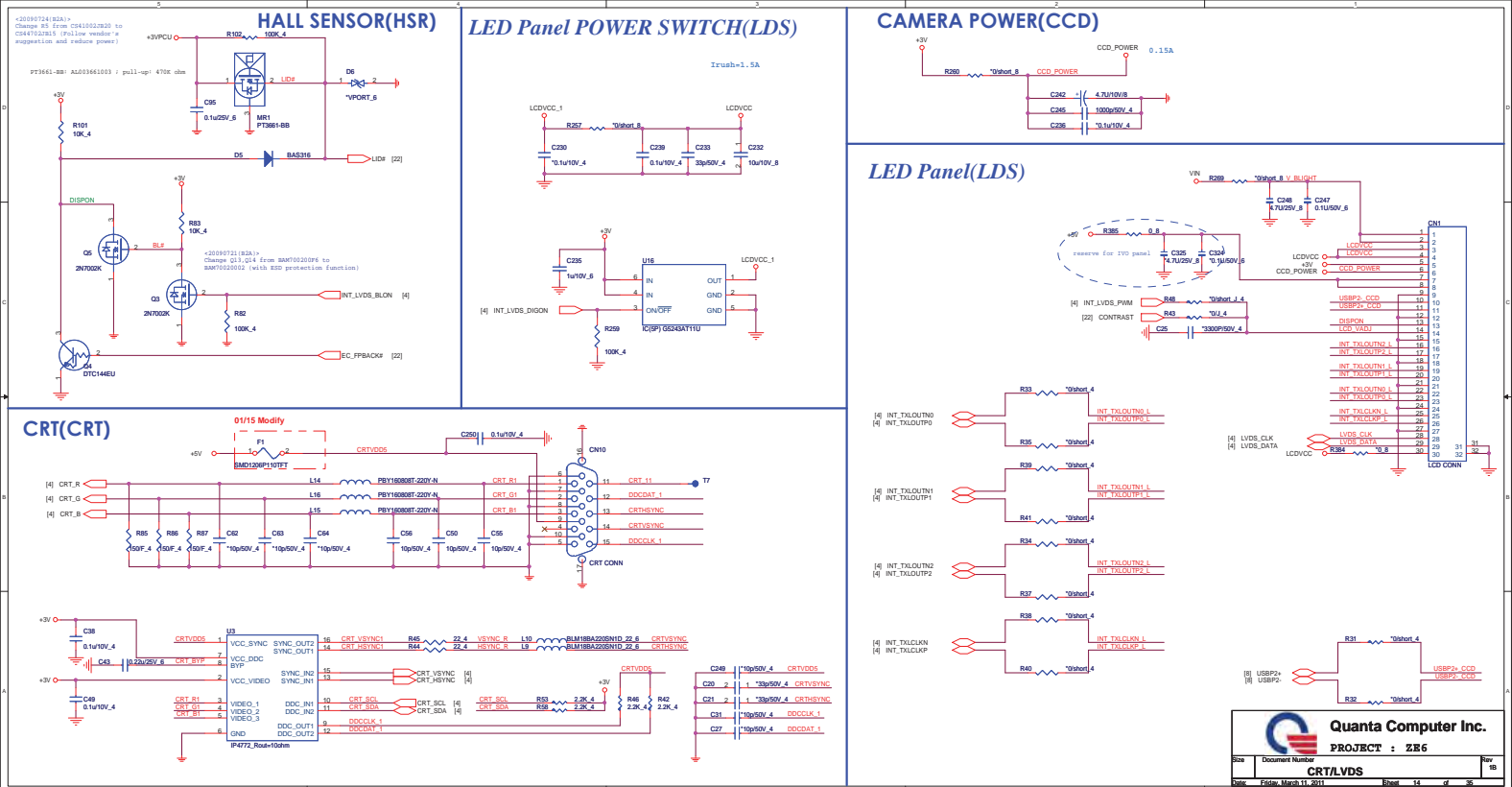


1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

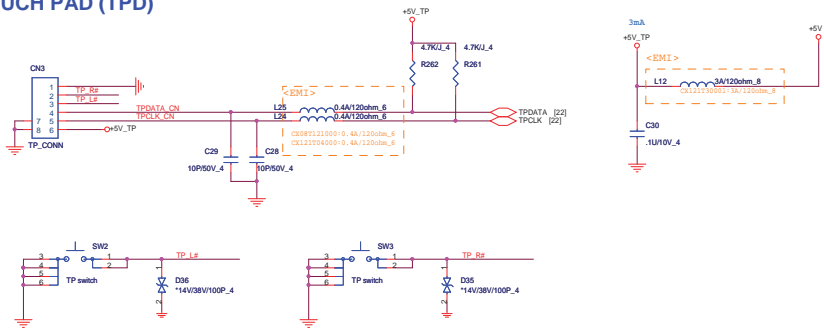


Quanta Computer Inc.
PROJECT : ZE6

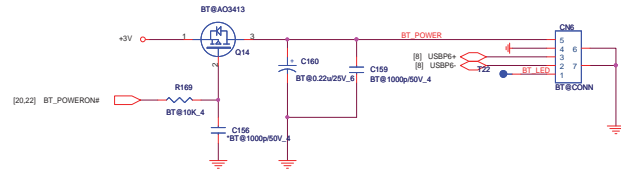
Size	Document Number	Rev
	TigerPoint GND	1B
Date:	Friday, March 11, 2011	Sheet 13 of 35



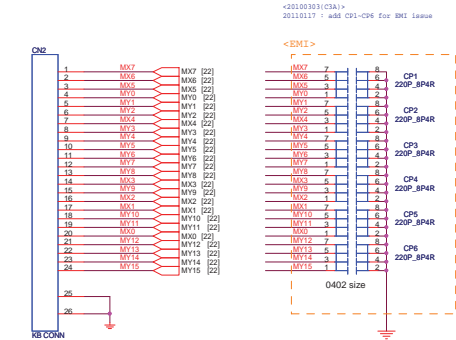
TOUCH PAD (TPD)



BLUETOOTH(BTM)

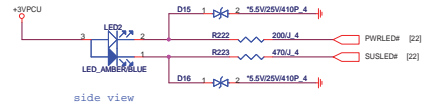


KEYBOARD (KBC)

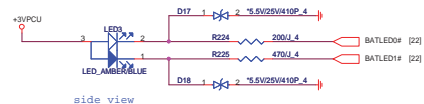


LED/SW (UIF)

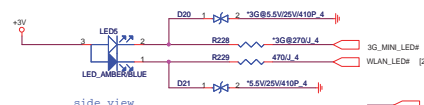
PWR LED
SUS LED



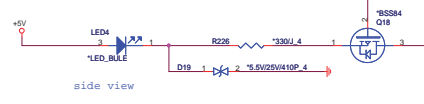
FULL LED
CHG LED



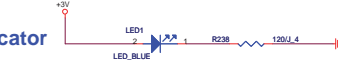
3G LED
WLAN LED



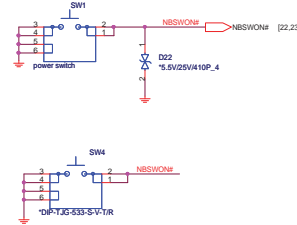
HDD LED



PWR indicator



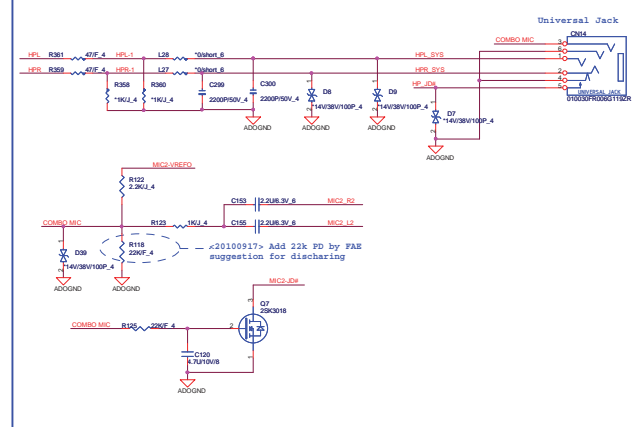
PWR Button



W/O 3G: use BE0R0083200
W 3G: use BEB00023A0

<20090609(A1A)> Checklist Rev1.0>
Need the buffer for LED driving
capability since the IOL is 6mA only.

HEADPHONE

[illegible][illegible]

Demodulation Filter L17 Place close to Codec

5V

DIGITAL

ANALOG

1.17

0.8

+5V/A

The schematic diagram shows the power supply section of the ADI-PMU. A +5V input is connected to a resistor network consisting of R184, R185, and R186. The output of this network is connected to the AMP_MUTEA pin [22] of the ADI-PMU. The diode network consists of D13, D14, and D12, which are connected to the AMP_MUTEA pin [22] and the AMP_MUTEB pin [23].

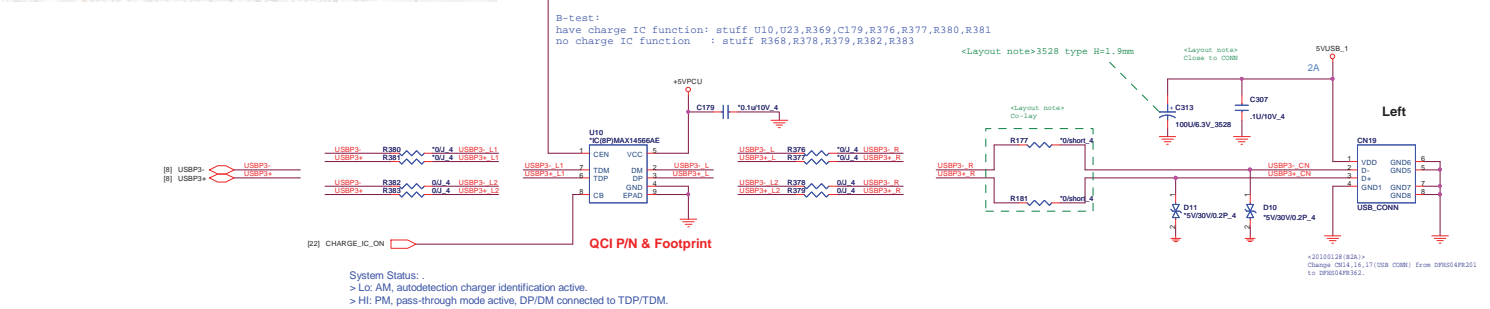


Enable USB Charger					
	AC	S4/S5	S4 (Battery < Setting%)	S4/S5	S4 (Battery < Setting%)
Charge Feature	O	O	O	O	X
Wake Feature	X		X		X

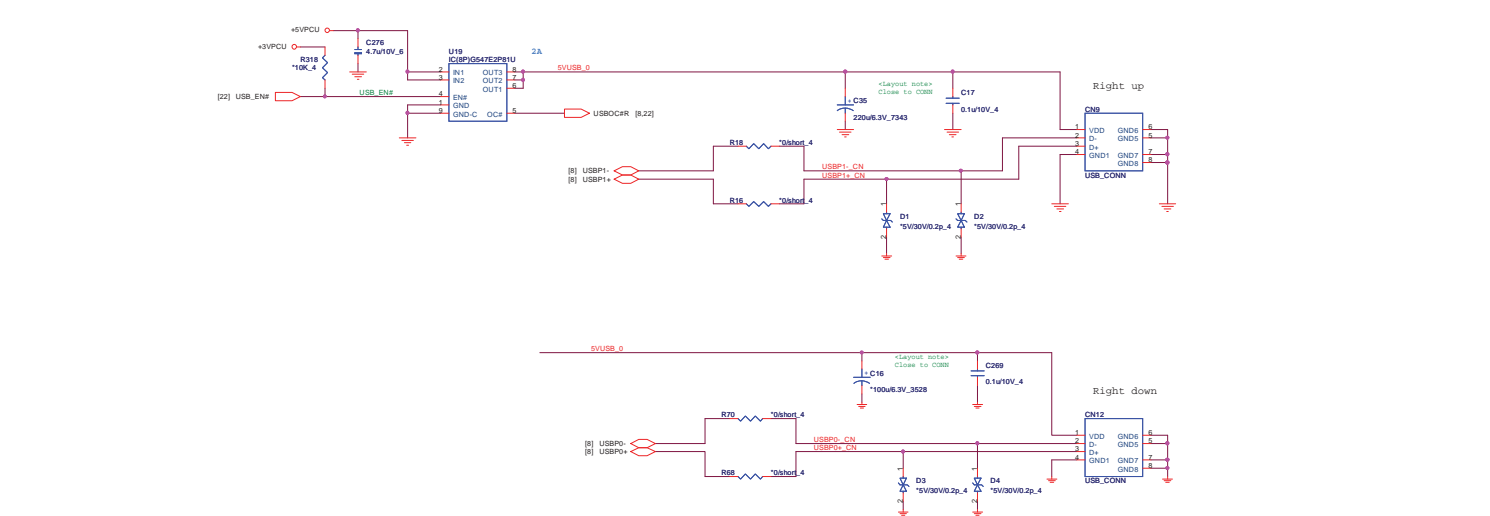
Disable USB Charger					
	AC	S4/S5	S4 (Battery < Setting%)	S4/S5	S4 (Battery < Setting%)
Charge Feature	O	X	Δ	X	X
Wake Feature	O		O		O

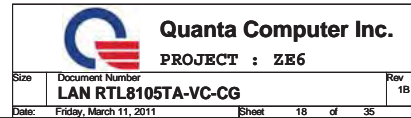
Note 1. Devices can be charged or not should same as other USB ports

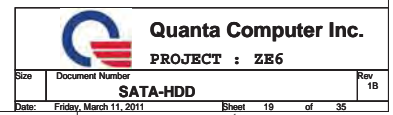
Note 1: Devices can be charged or not should same as other USB ports

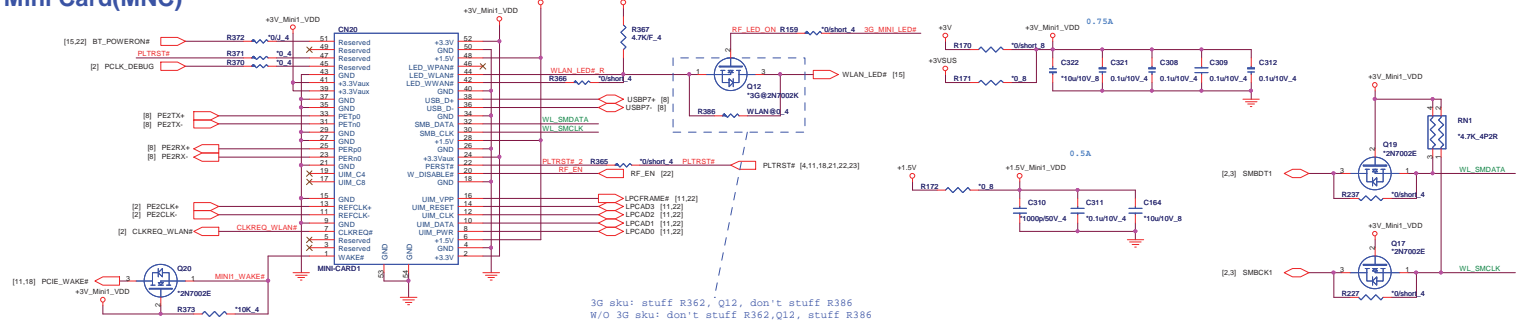


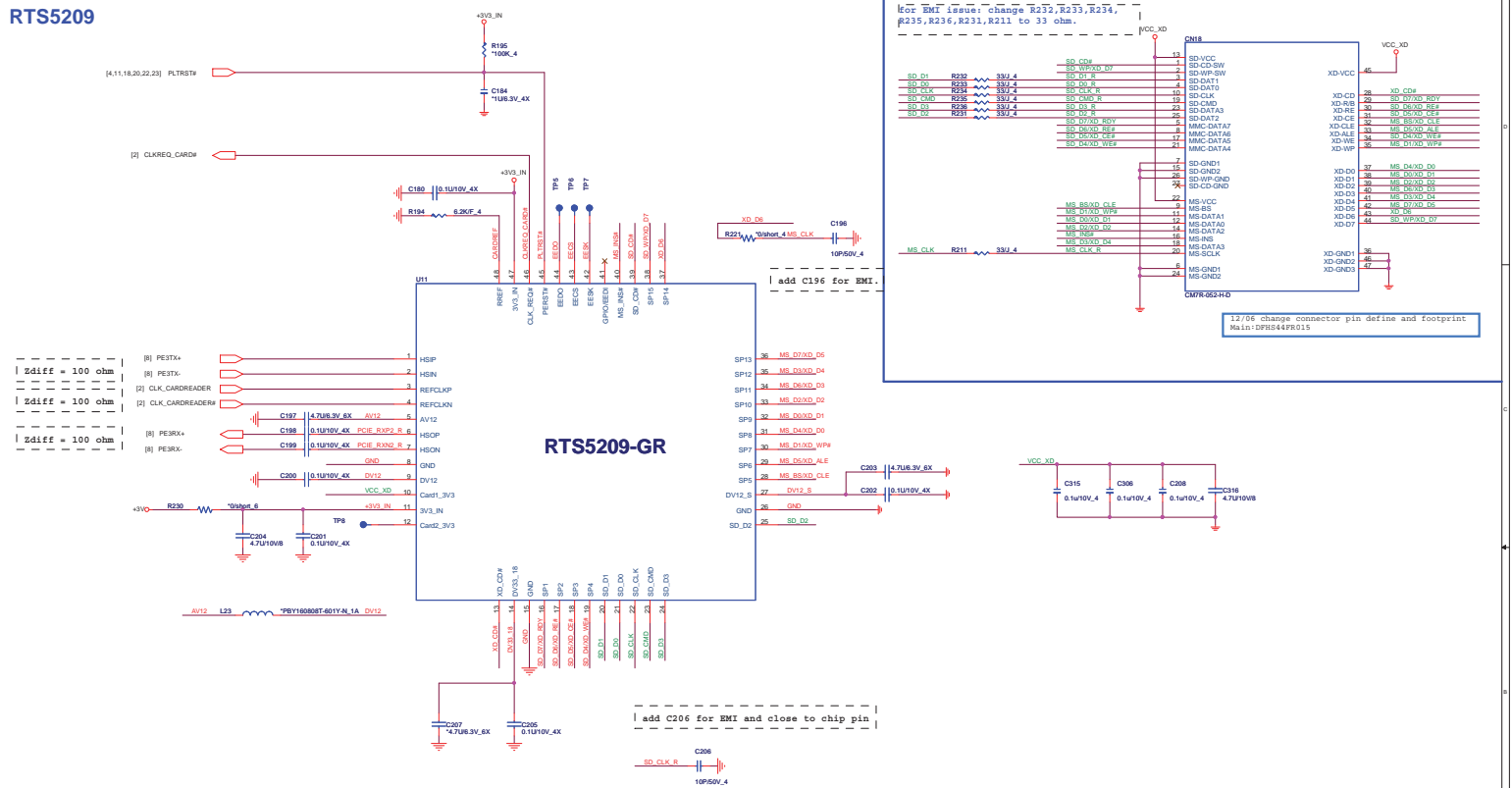
USB(USB)



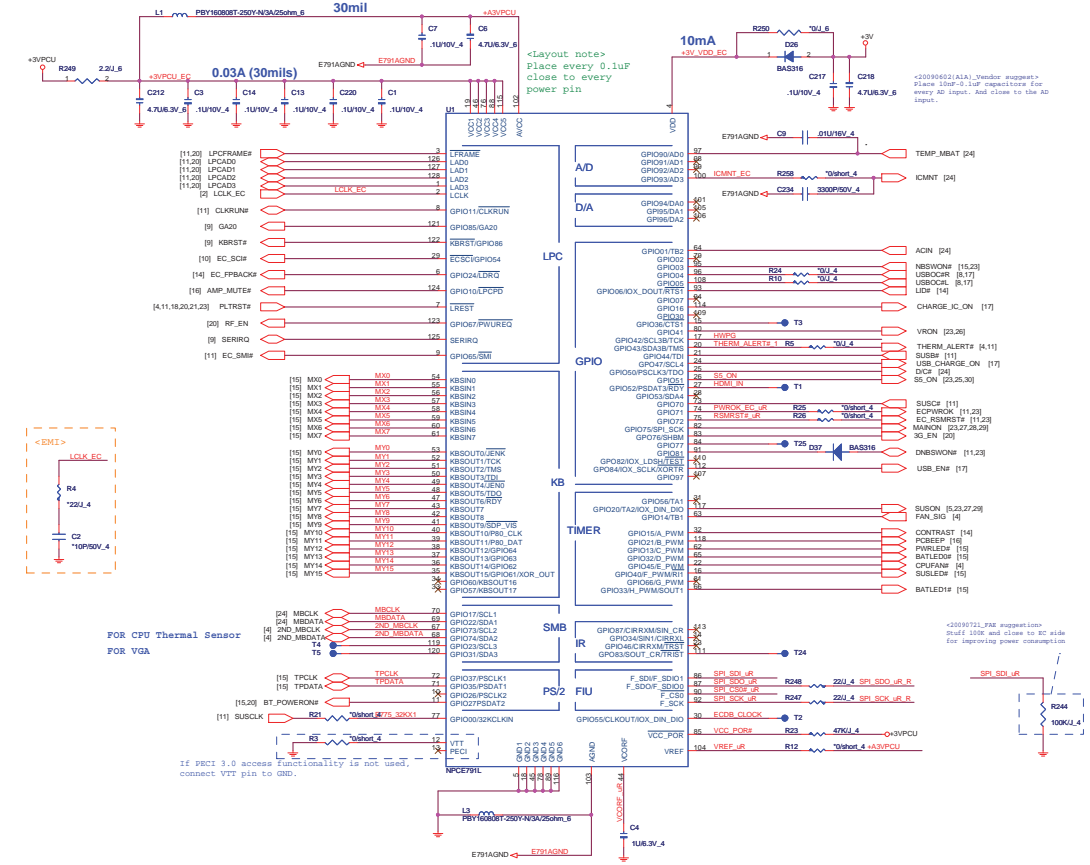




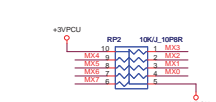




EC (KBC)



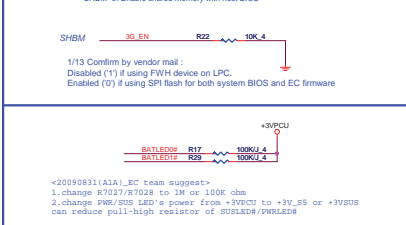
INTERNAL KEYBOARD STRIP SET (KBC)



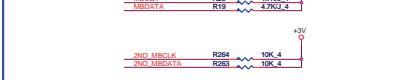
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	CPU thermal sensor

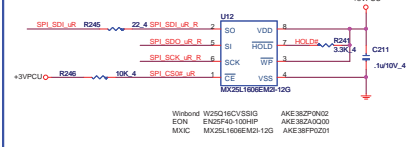
I/O ADDRESS SETTING (KBC)



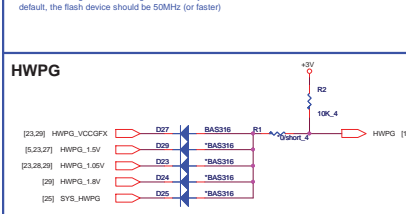
SM BUS PU(KBC)



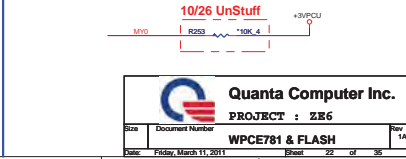
SPI FLASH(KBC)



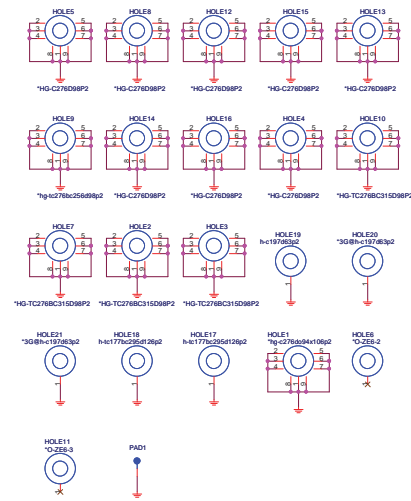
HWPG



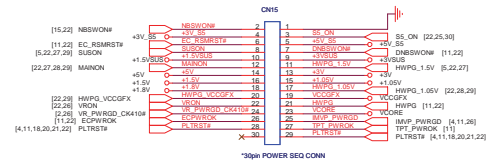
INTERNAL KEYBOARD STRIP SET(KBC)



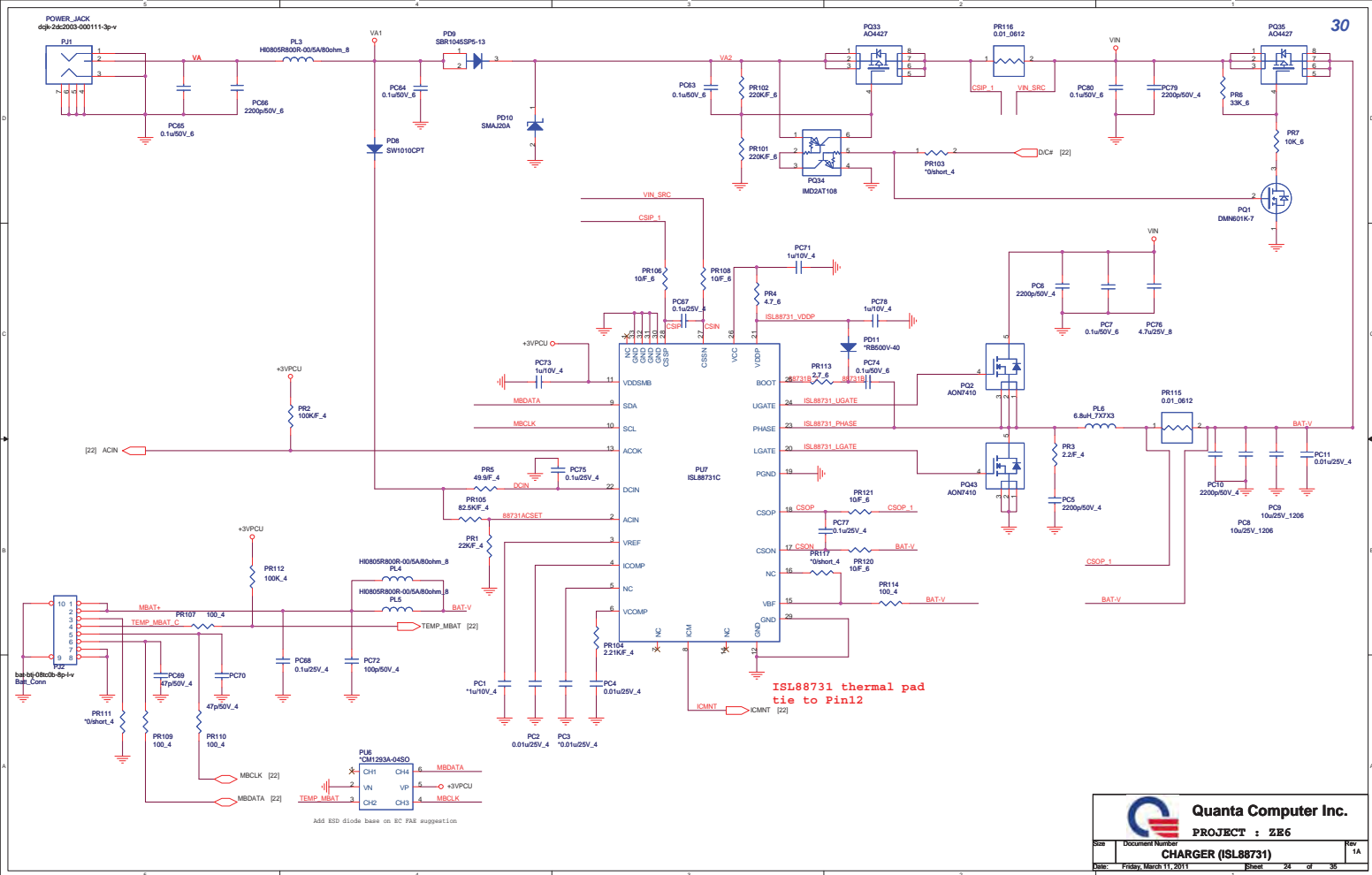
Hole

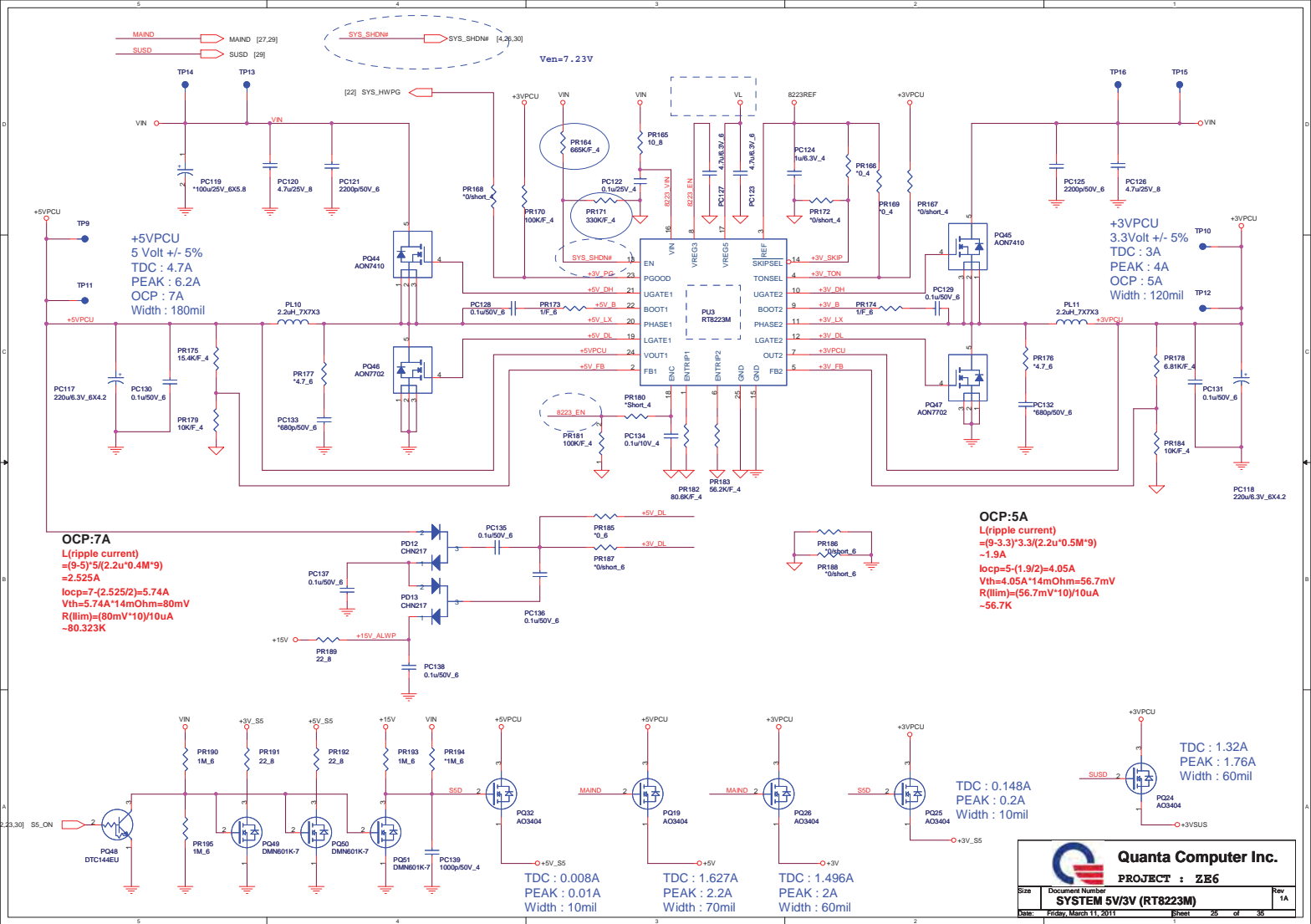


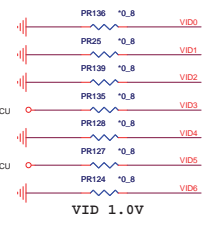
Power Sequence Connector 30pin (CPU)




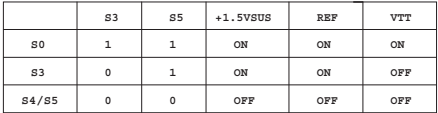
1	GND	11	HWPG1_1.5V	21	HWPG
2	NBSW0#	12	MAIN0N	22	VR0N
3	SS_ON	13	+3V	23	VCORE
4	+3V_SS	14	+5V	24	VR_PWRGD_CK410
5	+5V_SS	15	+1.05V	25	IMVP_PWRGD
6	EC_RST#RST#	16	+1.5V	26	ECFWRK
7	DNSW0N#	17	HWPG1_0.5V	27	TPT_PWR0K
8	SUS0N	18	+1.8V	28	RL_PWRGD
9	+3VSUS	19	VCC0K	29	PLTRST#
10	+1.5VSUS	20	HWPG_VCC0F#	30	RESERVE






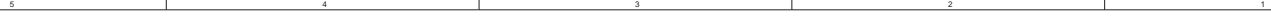


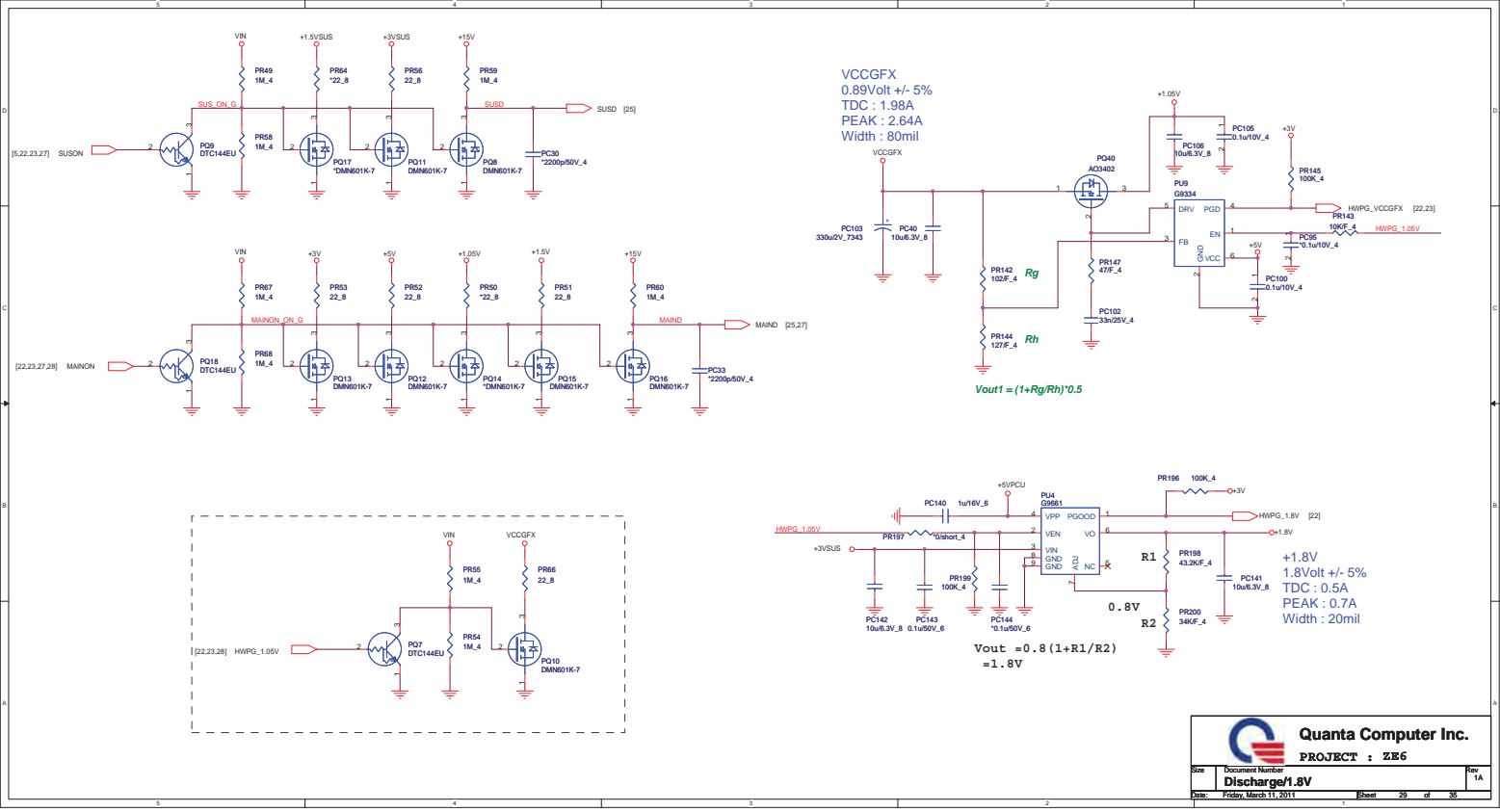
 Quanta Computer Inc. PROJECT : ZE6		Rev 1A
Size	Document Number VCore(IMAX8796GTJ+)	
Date:	Friday, March 11, 2011	Sheet 26 of 35

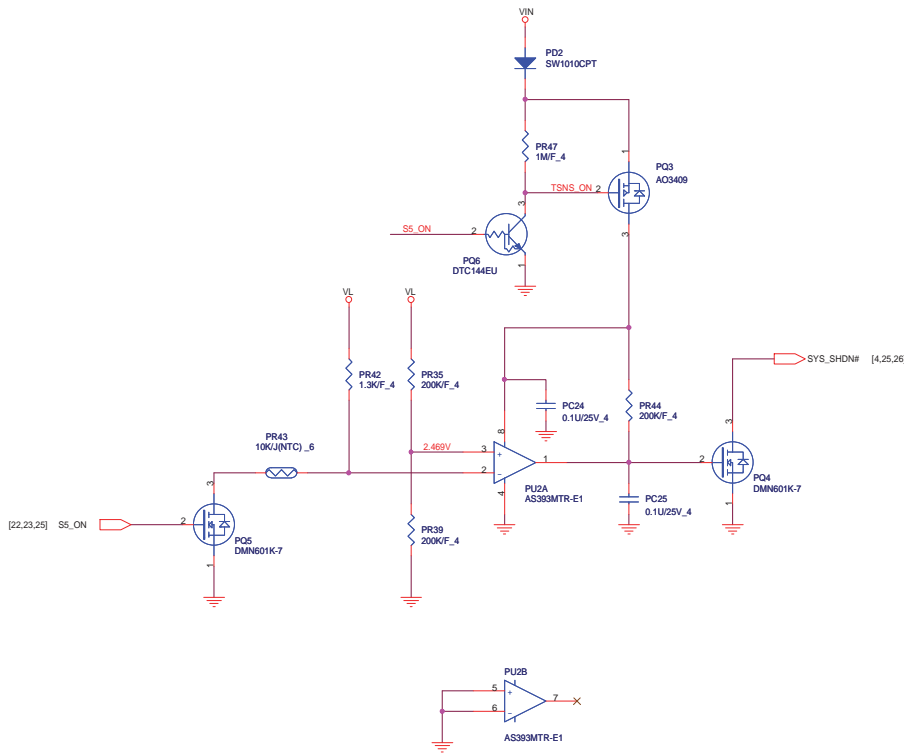



	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

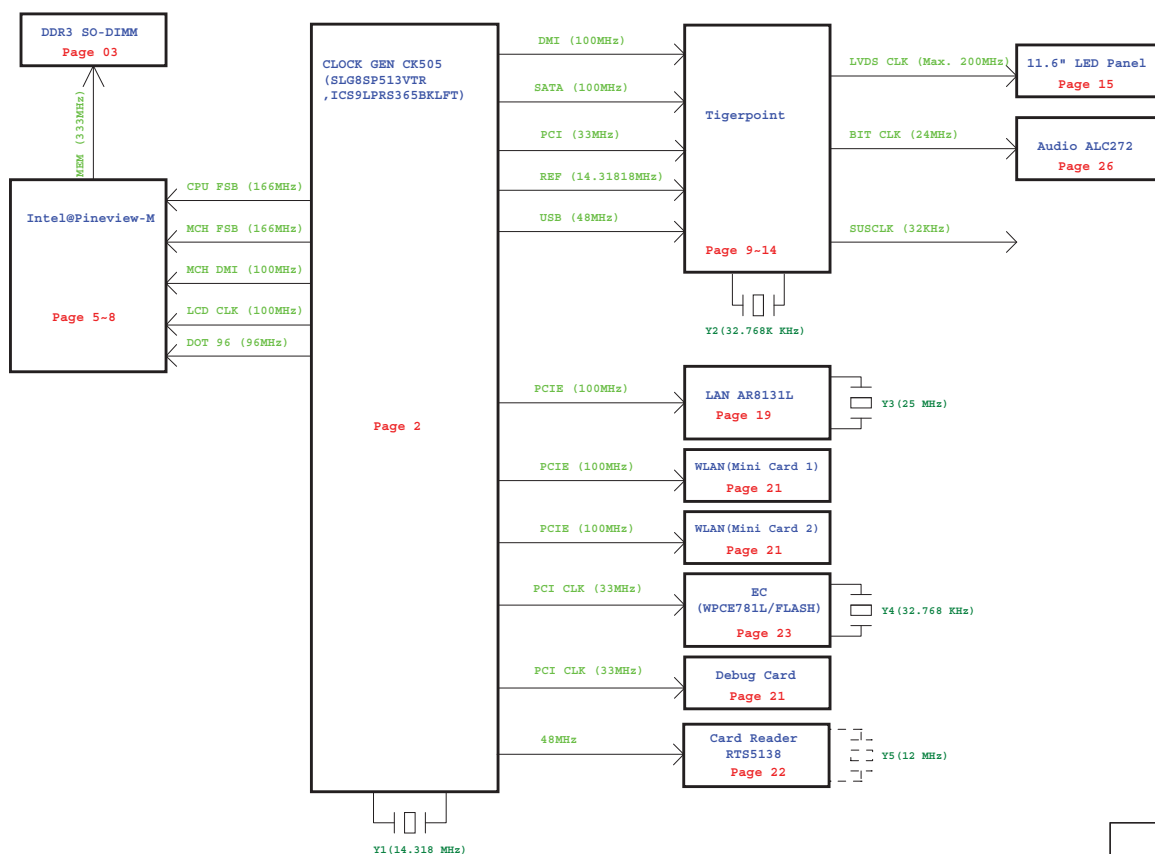
 Quanta Computer Inc. PROJECT : ZE6		
Size	Document Number DDR 1.5V(TPS51116)	Rev 1A
Date:	Friday, March 11, 2011	Sheet 27 of 35

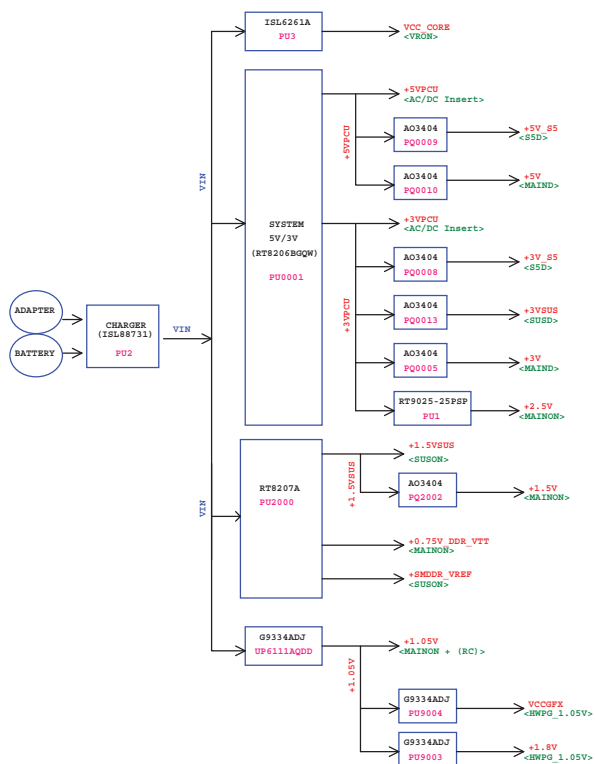




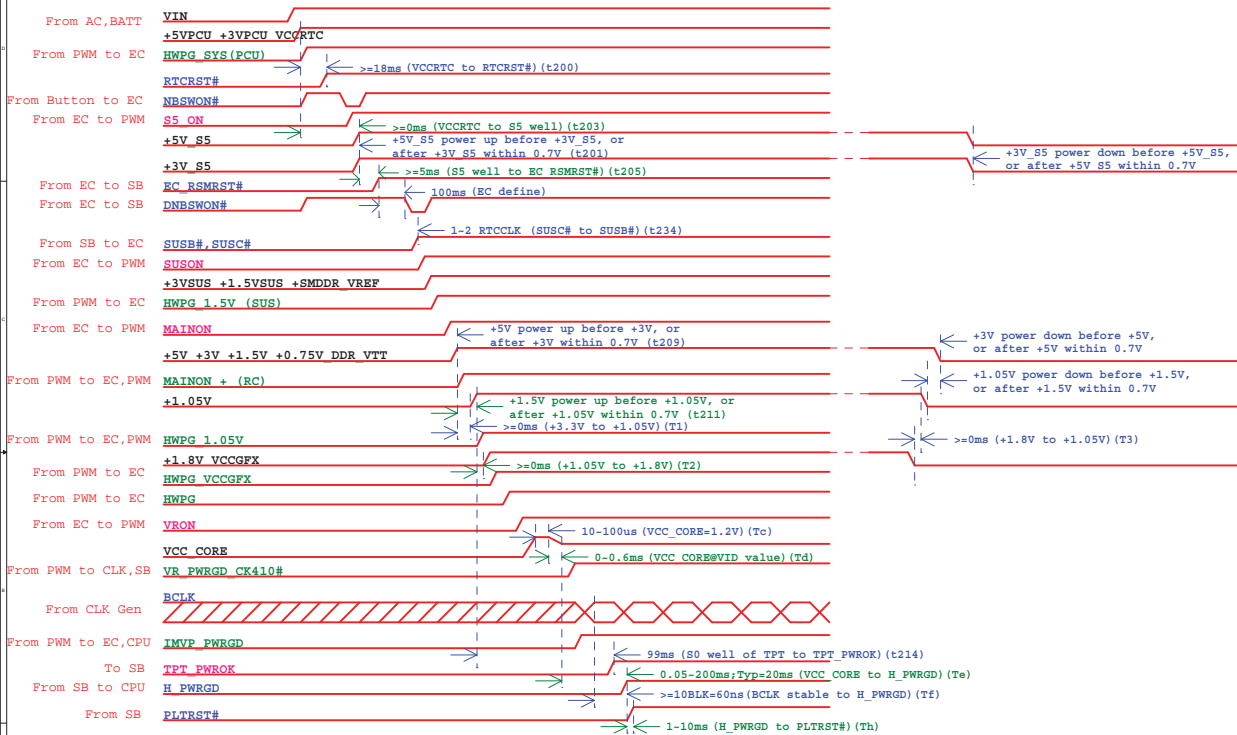


 Quanta Computer Inc.			
PROJECT : ZE6			
Size	Document Number	Rev	
Thermal protect		1A	
Date:	Friday, March 11, 2011	Sheet	30 of 35





POWER	Distribution
VIN	LCD Backlight
VCC_CORE	CPU
+5V9VDC	USB Connector
+5V_S5	TPT, TPT
+5V	TPT, CRT, TouchPad, Codec, SATA, FAN, HDMI
+3V9VDC	RTC, Hall Sensor, Light Sensor, EC, BIOS
+3V_S5	TPT, LAN, LAN EEPROM, RJ45 LED
+3VSUS	3G
+3V	CLK_GEN, CPU, TPT, LCD, CCD, DMIC, BT, Codec, WLAN/Wimax, Card reader, EC, DDR, HDMI
+1.5VSUS	DDR
+1.8V	CPU, HDMI
+1.5V	CPU, TPT
+0.75V_DDR_VTT	DDR
+SMDR_VREF	CPU, DDR
+1.05V	CLK_GEN, CPU, TPT
VCCGFX	CPU
+2.5V	HDMI



*Note: EC will sampling SUSB# & SUSC# every 5ms.

ICH SMBUS Table

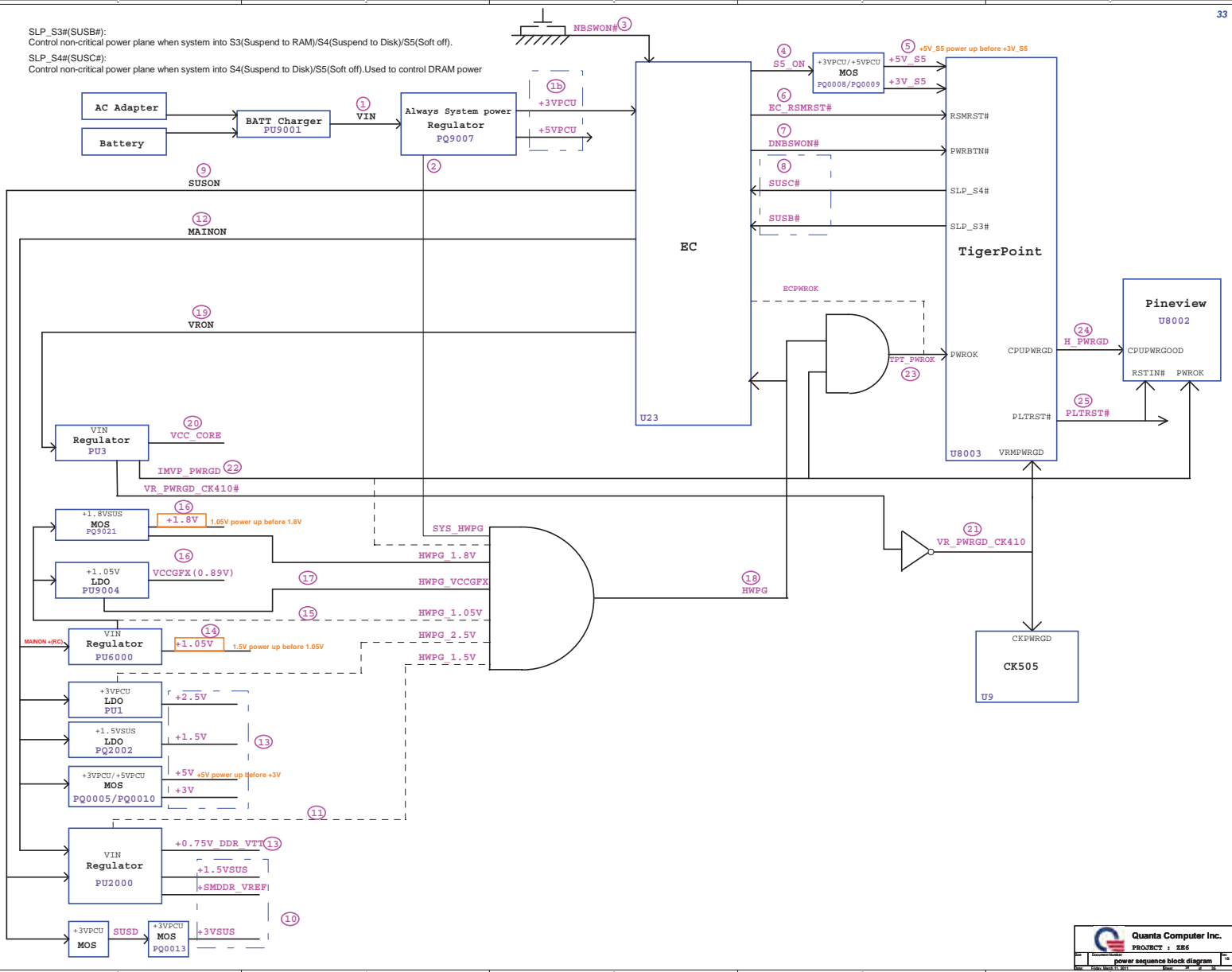
	CLK GEN	RAM	Mini Card (WLAN)	Mini Card (3G)
(SMB_DATA)/(SMB_CLK) (+3V_S5)	V	V	V	V
Power Plane	+3V	+3V	+3V	+3V_SUS
MOS CKT (Level shift)	Stuff	Stuff	*Reserve	Stuff

*Reserve: There is not SMBUS function in AVL

EC SMBUS Table

	Battery	CPU thermal Sensor	
EC781 SDA1 / SCL1 (+3VPCU)	V		
EC781 SDA2 / SCL2 (+3V)		V	
EC781 SDA3 / SCL3 (+3VPCU)			
Power Plane	+3VPCU	+3V	
MOS CKT (Level shift)	X	X	

SLP_S3#(SUSB#):
Control non-critical power plane when system into S3(Suspend to RAM)/S4(Suspend to Disk)/S5(Soft off).
SLP_S4#(SUSC#):
Control non-critical power plane when system into S4(Suspend to Disk)/S5(Soft off).Used to control DRAM power



Model		CHANGE LIST				MODEL	ZE6		
		REV					FROM	To	
ZE6 MB	A1	FIRST RELEASED: (PCB:A)					X	1A	
		Page 2 : add R374 for CLK GEN change version							
		Page 11 : change RTC connector type from SMT to holder.							
		Page 15 : modify TP connector pin define							
		Page 16 : modify audio and mic connector pin define.							
		Page 17 : modify USB charger IC circuit to support or not support charger function.							
	B	Page 29 : modify 1.8V IC enable signal to HWPFG_1.05V							
		20110117 Page 15 : add CPL-CP6 for EMI issue							
		20110117 Page 15 : for EMI issue: change R232,R233,R234,R235,R236,R231,R211 to bead CX5BB121001							
		20110118 Page 27 : for EMI issue: add PC96 ,PC32 and stuff PR48, PC29							
		20110118 Page 30 : Thermal temperature setting at 75C, change PR42 from 1.54K/F to 1.3K/F							
		20110131 Page 14 : add 5V into LCD connector for IVO panel to use.							
	B								
		1D							

DOC NO.	PROJECT MODEL :	11.6	APPROVED BY:		DATE:	2009/12/05
	PART NUMBER:		DRAWING BY:		REVISION:	1B



Quanta Computer Inc.
PROJECT : ZE6

Size

Document Number

Change list

Date: Friday, March 11, 2011

Rev 1B

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